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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/844,624	04/26/2001	Paul Richard Woods	10003959-1	2408

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AGILENT TECHNOLOGIES
INTELLECTUAL PROPERTY ADMINISTRATION
LEGAL DEPT., MS DL429
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EXAMINER	
MYERS, PAUL R	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 02/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/844,624	WOODS ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-14,16 and 18-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-14,16 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

In regards to applicants argument that Maeda does not teach the newly added feature of the switched power area being manufactured with a sub-micron semiconductor manufacturing process: Maeda is silent upon the manufacturing process of his system. It would be obvious to manufacture Maeda's system with a sub-micron manufacturing process. However, since Walsh et al teaches all the features for which Maeda was applied and a sub-micron manufacturing process, Maeda will be replaced with Walsh et al.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walsh et al PN 5,832,281 in view of Hidehiko et al JP06052070A.

3. In regards to claims 1, 5, 13, 18: Walsh et al teaches a circuit comprising: a constant power area (920B Column 88 lines 42-48) that receives constant power; a switched power area (the rest of the system 100 Column 88 lines 42-48) that receives interruptible power; wherein the

switched power area includes an input for receiving a normal mode clock signal (clock) and at least one transistor that is manufactured with a sub-micron semiconductor manufacturing process (column 13 lines 13-17); and an inactive state power reduction manager (920B) disposed in the constant power area (920B) for receiving a sleep signal (signal from suspend/resume switch 32), for performing a state save and for asserting a power control signal (0 volt suspend) that is used to disconnect the switched power area from a power supply (172). Walsh et al also expressly teaches stopping the clock (both stopping the clock and alternatively stopping the oscillator for the clock OSCOFF) Walsh et al does not teach the state save being a scan-based state save. Hidehiko teaches the use of a scan-based state-save and restore of data in a circuit upon power source discontinuation. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a scan-bases state-save as the state save in Walsh et al because this would have provided a fast method of data evacuation.

In regards to claims 2, 19: Walsh et al teaches a power switch (28 or alternatively any of the power switches in 170) attached to the inactive state power reduction manager (920B).

In regards to claim 3: Walsh et al shows power switches in figure 20 including FET switches.

In regards to claims 4, 14: Hidehiko teaches scan control for signals for controlling the scan based state save.

In regards to claim 6: Walsh et al teaches the wake up signal being an external signal.

In regards to claim 7: Walsh et al teaches the wake up signal being provided by a human trigger.

In regards to claims 8, 16, 20: Walsh et al teaches a memory storing the state information, including reading and writing.

In regards to claim 9: Walsh et al the memory storing the state information is a non-volatile memory.

In regards to claim 11: Walsh et al the memory storing the state information is in one of the constant powered area or the switched power area.

In regards to claim 12: Walsh et al teaches a board level circuit.

In regards to claims 21-23: Walsh et al teaches receiving a wake up signal (resume signal from switch 32), and responsive thereto for deasserting the power control signal that is used to connect the switched power area to the power supply (172), for performing a state restore.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PRM
February 11, 2005

PAUL R. MYERS
PRIMARY EXAMINER